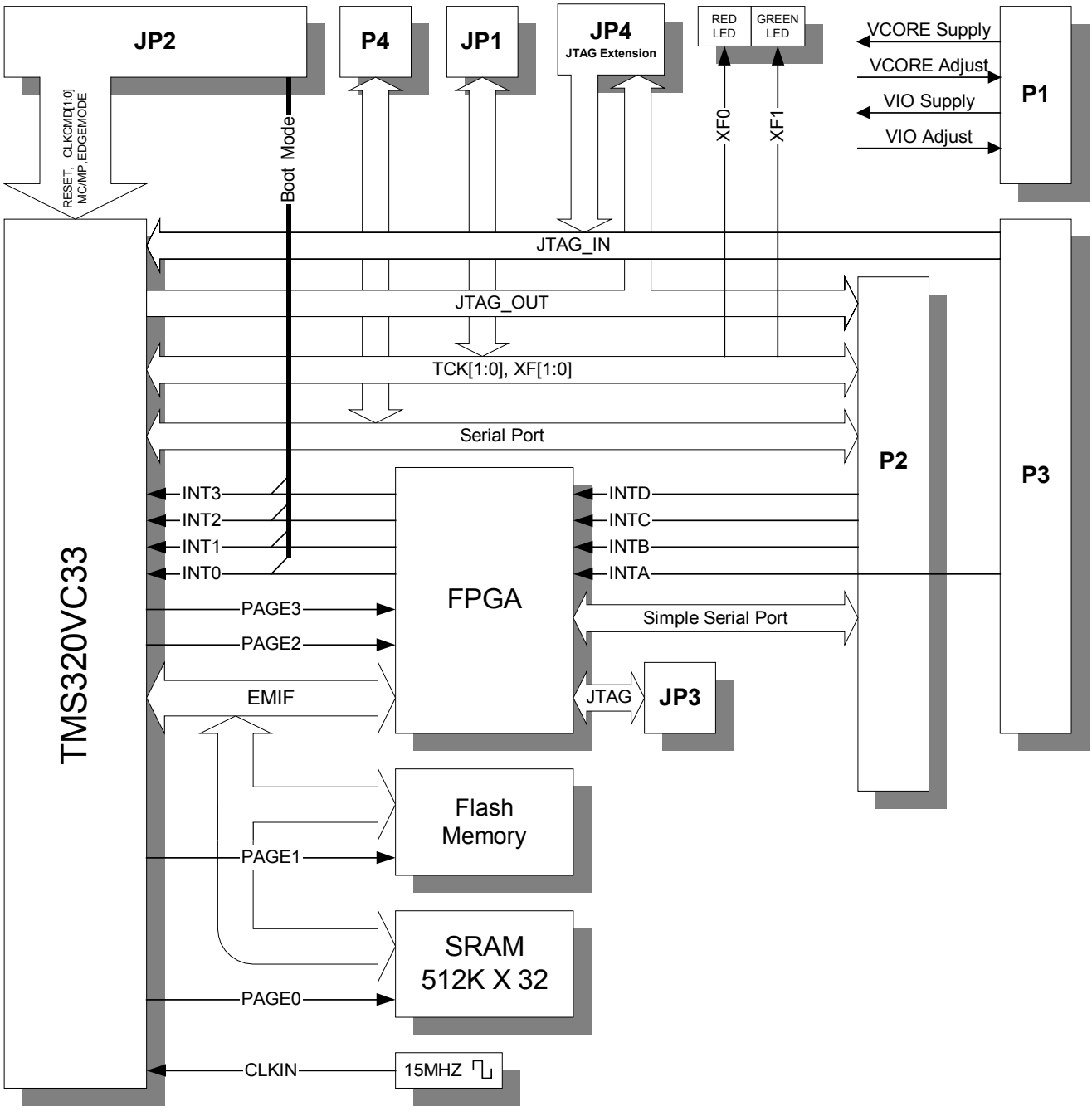
DSP RESEARCH

FleXDS Products

# FleXDS Module DSP-VC33-2M

# Block Diagram



# Specifications

- 2 Megabytes of 10ns, zero wait state SRAM, organized as 512K words X 32 bits
- Connector for serial port
- Socket for flash memory (AM29LV040 or equivalent)
- JTAG extension port, to connect multiple DSP targets together
- LEDs connected to XF0 and XF1
- Additional peripherals to support VC33 boot modes and DSP Research Audio I/O Module

# Installation

The module is installed onto the FleXDS host board connectors P6, P7 and P8, with JP2 and JP4 facing the top of the board. **Be sure to observe all ESD procedures** while handling the FleXDS host, VC33 module or any IO module installed on the FleXDS host.

# External Memory Map

The following tables detail the external memory map for the FleXDS-DSP-VC33-2M module. The address bits A21 to A23 are not wired to the SRAM nor are A19 to A23 connected to the flash memory. No external address bits are used to decode the peripherals Page2 and Page3 Registers. The consequence is that the memory, or registers, will be aliased within their respective page decode spaces. The term alias is defined as "*the same locations in a memory space can be accessed by two or more different address values*". The aliased address space is not displayed on the following maps.

Each page decode space is 8M words in length. External memory and page decode strobes are not active during TMS320VC33 internal accesses.

**MCBL/MC = 0**

| Page Decode | Address Range | Description |
|---|---|---|
| 0 | 0x0000 0000 to 0x001F FFFF | SRAM, 10ns access (zero wait state) |
| 1 | 0x0040 0000 to 0x0007 FFFF | Flash memory |
| 2 | 0x0080 0000 to 0x0080 9FFF | TMS320VC33 internal access |
| 2 | 0x00BF FFFF | Page 2 Peripheral Register |
| 3 | 0x00FF FFFF | Page 3 Peripheral Register |

**MCBL/MC = 1**

| Page Decode | Address Range | Description |
|---|---|---|
| 0 | 0x0000 0000 to 0x0000 0FFF | TMS320VC33 internal access |
| 0 | 0x0000 1000 | Boot 1 vector, TMS320VC33 internal access |
| 0 | 0x0000 1001 to 0x001F FFFF | SRAM, 10ns access (zero wait state) |
| 1 | 0x0040 0000 | Boot 2 vector, TMS320VC33 internal access |
| 1 | 0x0040 0001 to 0x007F FFFF | Flash memory |
| 2 | 0x0080 0000 to 0x0080 9FFF | TMS320VC33 internal access |
| 2 | 0x00BF FFFF | Page 2 Peripheral Register |
| 3 | 0x00FF F000 | Boot 3 vector, TMS320VC33 internal access |
| 3 | 0x00FF FFFF | Page 3 Peripheral Register |

# Configuration

## Boot, Interrupt and DSPR Audio I/O Module Support

An additional peripheral has been implemented with a programmable generic array logic chip (GAL) on the VC33 FleXDS module. The GAL satisfies two requirements for the VC33 module. The first is to control the activity on the interrupt pins at reset, so that the boot mode may be entered into the VC33. After reset, the external interrupts are then enabled under software control. The second is to provide a second serial port to control a codec located on the FleXDS Audio module. This port has been implemented as a simple "bit-banger" type of serial port, where all signals are under software control.

Inside the GAL are two registers. One register is addressed when the TMS320VC33 PAGE2 address decode output is active, the other when the PAGE3 address decode output is active. These two registers are referred to as the Page2 and Page3 registers. The Page2 register will be chosen when any address between 0x00 800000 and 0x00BFFFFF and the external memory strobe is active. The Page3 register will be chosen when any address between 0x00C00000 and 0x00FFFFFF and the external memory strobe is active.

# Page2 and Page3 Register Description

### Page2 Register Write

**D0: Codec Reset, active LOW**

This output of this bit is connected to the Codec reset pin when the Audio module is installed. While this bit is '0', the codec is held in the RESET condition. When this bit is set to '1', the codec will be ready to process data. The initial condition after a power up or Flying Reset is '0', codec reset active.

**D1: Interrupt Enable, active HIGH**

This bit controls the access to the Interrupt pins on the VC33. While this bit is '0', external interrupts are blocked, and the levels on all the VC33 interrupt pins are controlled by jumpers located on JP2. The levels on the VC33 interrupt pins after reset determine the boot mode. After this bit has been set '1' under program control, the external interrupts are enabled onto the VC33 interrupt pins. The initial condition after a power up or Flying Reset is '0', interrupts disabled. The state of this pin can be probed at TP3 on the VC33 module.

### Page2 Register Read

There is no data that can be read back from the Page2 Register.

### Page3 Register Write

**D0: Codec Control Serial Data Out**

This output of this bit is connected to the Codec Control Data Input pin when the Audio module is installed. Codec data must be valid on the falling edge of the codec clock.

**D1: Codec Control Serial Clock Out**

This bit is connected to the Codec Control Clock input of the codec when the Audio module is installed. The control clock is generated by software. Data will be clocked into the codec on the falling edge (writing a '0' to this bit) and clocked out of the codec on the rising edge (writing a '1' to this bit). The initial condition after a power up or Flying Reset is '0'.

**D2: Codec Control Sync Out**

This bit is connected to the Codec Control Sync input of the codec when the Audio module is installed. Setting this bit high one clock before the first data bit and low at the first data bit generates the control sync. The control sync input is sampled every falling edge of the codec clock. The initial condition after a power up or Flying Reset is '0'.

### Page3 Register Read

**D0: Codec Status Serial Data In**

This bit originates from the Codec Control Data Output pin when the Audio module is installed. Because data is not latched, the codec clock must be stable before reading this bit. Data will be valid out of the codec after the rising edge of the codec clock.

The Audio Module uses Interrupt 0. The Interrupt Enable bit in the Page2 Register must be set to '1' to poll or use this interrupt.

For a detailed explanation of codec part used on the DSPR Audio I/O Module, see the Crystal Semiconductor CS4218 16-bit Stereo Audio Codec data sheet (www.cirrus.com).

# Jumpers

**JP1**

| | |
|---|---|
| 1-2 | INT2_L Pull Up. When this jumper is installed, Interrupt 2 is pulled up through a 10K resistor to 3.3V. This position must be vacant if a jumper is installed from pin 3 to 4. |
| 3-4 | INT2_L Pull Down. When this jumper is installed, Interrupt 2 is pulled down through a 10K resistor to ground. This position must be vacant if a jumper is installed from pin 1 to 2. |
| 5-6 | INT0_L Pull Up. When this jumper is installed, Interrupt 0 is pulled up through a 10K resistor to 3.3V. This position must be vacant if a jumper is installed from pin 7 to 8. |
| 7-8 | INT0_L Pull Down. When this jumper is installed, Interrupt 0 is pulled down through a 10K resistor to ground. This position must be vacant if a jumper is installed from pin 5 to 6. |
| 9-10 | INT1_L Pull Up. When this jumper is installed, Interrupt 1 is pulled up through a 10K resistor to 3.3V. This position must be vacant if a jumper is installed from pin 11to 12. |
| 11-12 | INT1_L Pull Down. When this jumper is installed, Interrupt 1 is pulled down through a 10K resistor to ground. This position must be vacant if a jumper is installed from pin 9 to 10. |
| 13-14 | INT3_L Pull Up. When this jumper is installed, Interrupt 3 is pulled up through a 10K resistor to 3.3V. This position must be vacant if a jumper is installed from pin 15 to 16. |
| 15-16 | INT3_L Pull Down. When this jumper is installed, Interrupt 3 is pulled down through a 10K resistor to ground. This position must be vacant if a jumper is installed from pin 13 to 14. |
| 17-18 | CLKMD0 Pull down, used to configure CPU clock speed. See data sheet for pin explanation. If not installed CLKMD0 is pulled up to 3.3V through a 10K resistor. |
| 19-20 | CLKMD1 Pull down, used to configure CPU clock speed. See data sheet for pin explanation. If not installed CLKMD1 is pulled up to 3.3V through a 10K resistor. |
| 21-22 | SHZ Pull down, used to tri-state the DSP. See data sheet for pin explanation. If not installed SHZ is pulled up to 3.3V through a 10K resistor. |
| 23-24 | MCB/MP Pull down, used to put the DSP in either the microcomputer or microprocessor mode. See data sheet for pin explanation. If not installed MCB/MP is pulled up to 3.3V through a 10K resistor. |
| 25-26 | EDGEMODE Pull down, used to set the DSP interrupt mode. See data sheet for pin explanation. If not installed MCB/MP is pulled up to 3.3V through a 10K resistor. |
| 27-28 | Last DSP On JTAG Loop Select. This setting is used in conjunction with the JTAG expansion connector, JP4. When this jumper is installed, the VC33 board is configured as the last DSP in a multi-board JTAG loop and JP4 is not functional. When the jumper is not installed, JP4 becomes active, so that additional boards may be daisy-chained on a JTAG loop. |
| 29 | Not Connected |
| 30 | External DSP Reset, active LOW |

# Connectors

### P4 - Serial Port

| | |
|---|---|
| 2, 4, 6, 8, 10, 12, 14 | Ground |
| 1 | Not connected |
| 3 | Serial port CLKX0 |
| 5 | Serial port DX0 |
| 7 | Serial port FSX0 |
| 9 | Serial port CLKR0 |
| 11 | Serial port DR0 |
| 13 | Serial port FSR0 |

### JP1 – Miscellaneous I/O

| | |
|---|---|
| 1,3,5,7,9 | Ground |
| 2 | XF0 |
| 4 | XF1 |
| 6 | TCK0 |
| 8 | TCK1 |
| 10 | IACK_L |

### JP3 – U2 ispGAL22LV10 Programming Pins

| | |
|---|---|
| 1 | 3.3V |
| 2 | TDO |
| 3 | TDI |
| 4 | Reserved |
| 5 | Reserved |
| 6 | TMS |
| 7 | Ground |
| 8 | TCK |

## JP4 – JTAG Expansion Connector

| | |
|---|---|
| 4, 6, 8, 10, 12 | Ground |
| 1 | TMS |
| 2 | TRST |
| 3 | TDI |
| 5 | No connection |
| 7 | TDO |
| 9 | TCK_RET |
| 11 | TCK |
| 13 | EMU0 |
| 14 | EMU1 |

### How to use the JTAG Expansion Port

The JTAG expansion port is to be connected to another standard JTAG target connector, such as P9 on a FleXDS Host board. Two standard 14 pin connectors with ribbon cable may be used. The cable must connect pin 1 of the expansion port to pin 1 of the target port, and so on through all 14 pins. The last DSP jumper is removed for all VC33 modules except the last target (if another FleXDS module).

**CAUTION:** This connector is **NOT KEYED** in order to avoid accidental connection of a JTAG pod. **OBSERVE PIN 1 POLARITY** when connecting multiple boards. **DAMAGE WILL OCCUR** if the cable is connected to another board's JTAG expansion port, or is incorrectly installed to a target. Keep cable length as short as possible.

# Contact and Service Information

For further information or service contact:

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# References

## DSP Research Publications (www.flexds.com)

Schematic for the FleXDS-VC33-2M DSP Module

Schematic for the Peripheral GAL, U2

Parts List for the FleXDS-VC33-2M DSP Module

Layout for the FleXDS-VC33-2M DSP Module

## Texas Instruments Publications: (www.ti.com)

TMS320VC33 Data Sheet (SPRS087)

TMS320C3x User's Guide (SPRU031)

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